REMARKS

In the present amendment, the specification and claims 1-5 have been amended, and claims 11-20 have been added. Thus, claims 1-5 and 11-20 are currently pending in the case. Further examination and reconsideration of the presently claimed application are respectfully requested.

Objection to the Specification

The specification was objected for an informality. In particular, the Office Action suggests that the "Applicant uses the term multiple byte-wise CRC circuit in various places throughout the specification, but nowhere in the Application [does] the Applicant teach what a multiple cyclic redundancy check circuit is" (Office Action, page 2). As set forth in more detail below, the objection to the specification is respectfully traversed.

The specification, as originally filed, does provide sufficient teaching for what is "a multiple byte-wise CRC circuit" and for what it does. For example, on page 3, the originally filed specification teaches that a CRC circuit is one that performs a CRC calculation on a data stream before and after transmission (of the data stream) to determine when errors are present in the data stream. Exemplary CRC circuits that perform bit-wise CRC calculations (i.e., a CRC calculation that is performed one bit at a time) are shown in Figs. 2 and 3, and described on pages 3-6 of the originally filed specification. As noted on pages 10-11 of the originally filed specification, the "present invention provides a system and method for performing a CRC calculation on multiple bytes of data in a single cycle." Such a system may be considered to perform a multiple-byte CRC calculation (e.g., a CRC calculation on eight bytes of data at a time). *See*, e.g., pages 16-17 of the originally-filed Specification. The system is further described as including "a first CRC module, a second CRC module and a decision module," although in some embodiments, the system may include "a total of eight CRC modules ... [where each] CRC module processes a different number of bytes ..." (*See*, e.g., page 10 of the originally-filed specification). Though the system is referred to throughout the originally-filed specification as a "multiple byte-wise CRC circuit," the specification inconsistently describes the circuit as including "multiple CRC circuits," one or more "CRC modules," and in more specific embodiments, as including, e.g., an "eight-byte CRC circuit," a "seven-byte CRC circuit," etc., on down to a "byte-wise CRC circuit."

For purposes of clarity and consistency, portions of the specification have been amended to describe the above-mentioned system as a "multiple-byte CRC circuit" having a "plurality of CRC modules," where each module is configured for performing a CRC calculation on a different number of bytes of data at a time (i.e., during a single cycle). For example, an eight-byte-wide CRC module may be included within the circuit for performing a CRC calculation on an eight-byte-wide segment of data; a seven-byte-wide CRC module may be included within the circuit for performing a CRC calculation on a seven-byte-wide segment of data, etc. Support for the amendments may be found in the specification (e.g., on pages 10-11 and 15-18) and the claims as originally filed. Therefore, the amendments to the specification do not introduce new matter. Accordingly, Applicants respectfully request removal of this objection.

Section 112, 1st Paragraph, Rejections

Claims 1-5 were rejected under 35 U.S.C. § 112, first paragraph, for multiple reasons. First, claims 1-5 were rejected for being based on a disclosure which is not enabling, per *In re Mayhew*, and more specifically, for the specification (allegedly) failing to "teach what a multiple byte-wise CRC circuit is." As noted above, Applicants believe that the originally-filed specification does, in fact, provide sufficient description for a multiple byte-wise CRC circuit by describing the circuit as one configured for "performing a CRC calculation on multiple bytes of data in a single cycle" (Specification, page 10). However, in order to expedite prosecution, portions of the originally-filed specification and claims have been amended to more clearly describe the "multiple-byte CRC circuit" as comprising a plurality of CRC modules, where each of the CRC modules is configured to perform a CRC calculation on a different number of bytes of data during a single cycle.

Claims 1-5 were further rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention. With regard to claim 1, the Examiner suggests that "[n]owhere in the specification does the Applicant teach a step for **providing** multiple cyclic redundancy check circuits as part of a method of performing a cyclic redundancy check calculation (Note: the step for **providing** multiple cyclic redundancy check circuits is generally a design and manufacture step whereby check circuits are deigned and built onto circuitry for providing error protection)." (Office Action, pages 3-4, emphasis original). Though the presently claimed step of providing multiple cyclic redundancy check (CRC) circuits is disclosed in the originally-filed specification (e.g., paragraph 29, pages 10-11) as part

of a method of performing a cyclic redundancy check calculation, Applicant's recognize that such a limitation is inconsistent with a method generally performed by a user of the CRC circuit. To expedite prosecution, claim 1 has been amended to replace the originally filed limitation of "providing multiple cyclic redundancy check circuits" with a limitation believed to be more consistent with a user-implemented method.

The amendments described above are believed to clarify the claim language in a manner that addresses the concerns expressed in the Office Action. Accordingly, Applicants respectfully request removal of this rejection.

Section 112, Second Paragraph, Rejections

Claims 1-5 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In addition, claims 1-5 were rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. (*See*, Office Action, pages 4-7). To expedite prosecution, claims 1, 4, and 5 have been amended in a manner which addresses the concerns expressed in the Office Action. Accordingly, Applicants respectfully request removal of this rejection.

Section 102 Rejections

Claims 1 and 3 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,282,215 to Hyodo et al. (hereinafter "Hyodo"). The standard for "anticipation" is one of fairly strict identity. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. Of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), MPEP 2131. Hyodo does not disclose all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

Hyodo fails to provide teaching or suggestion for a method of performing a cyclic redundancy check (CRC) calculation on a data stream, where the method includes: (i) supplying a data stream to a multiple-byte CRC circuit comprising a plurality of CRC modules, wherein each of the CRC modules is configured to perform the CRC calculation on a different number of bytes

of data during a single cycle, (ii) determining which one of the plurality of CRC modules should be used for processing a segment of data currently supplied to the multiple-byte CRC circuit, and (iii) after said step of determining, processing the segment of data using only the CRC module determined appropriate for the current segment of data. Amended independent claim 1 recites, in part:

> A method of performing a cyclic redundancy check (CRC) calculation on a data stream composed of one or more segments of data, the method comprising: supplying the data stream, one data segment per cycle, to a multiple-byte cyclic redundancy check (CRC) circuit comprising a plurality of CRC modules, wherein each of the CRC modules is configured to perform the CRC calculation on a different number of bytes of data during a single cycle; determining which one of the plurality of CRC modules should be used for processing a segment of data currently supplied to the multiple-byte CRC circuit; after said step of determining, processing the segment of data using only the CRC module determined appropriate for the current segment of data, wherein said step of processing comprises performing the CRC calculation on the current segment of data to produce CRC calculation results for the current cycle ...

Support for the amendments made to claim 1 may be found in the present specification, for example, on pages 10-11 and 15-18. For example, the specification discloses that each of the plurality of CRC modules may be configured to perform a CRC calculation on a different number of bytes of data during a single cycle. After determining which CRC module should be used for processing a segment of data, the method processes the segment of data using only the selected CRC module.

Hyodo discloses a "synchronization circuit [that] receives and holds in a bit serial manner the input bit trains ... performs a CRC operation in a bit serial manner on the held input bit trains by a continuous CRC arithmetic unit ... and performs the necessary synchronization control upon receiving the CRC arithmetic operation result at a synchronization control unit" (Hyodo, Abstract). The CRC arithmetic unit is shown in Fig. 3 of Hyodo as including a plurality of ROM tables (11) and a plurality of EX-OR logic gates (13) being connected in parallel as illustrated (*See*, e.g., Hyodo, column 4, line 57 to column 5, line 2). Hyodo further teaches that the "input bit train... is divided into suitable numbers of bits (shown by α_1, α_2... α_p, for example, each comprised of five bits). The CRC arithmetic operation result[s] read out from the corresponding ROM 11 ... are input to the EX-OR's 13 as illustrated ... [and the] CRC arithmetic operation result C_{out} is obtained from the final stage EX-OR 13." As such, the method disclosed by Hyodo appears to divide an input bit train into equal-length segments of data (e.g., five bits), each of which are input to a different one of the ROM tables. The CRC results obtained from the ROM tables (11) are input into the EX-OR logic gates (13) in a serial manner. For example, Fig. 3

shows how the result from a preceding EX-OR logic gate is input, along with one of the ROM table results, to the next EX-OR gate. The process continues until a final CRC arithmetic operation result (C_{out}) is obtained from the final stage EX-OR logic gate.

The process described by Hyodo is altogether different from the presently claimed method of performing a CRC calculation on a data stream. For example, the process described by Hyodo fails to include the presently claimed step of supplying a data stream to a multiple-byte cyclic redundancy check (CRC) circuit comprising a plurality of CRC modules, where each of the CRC modules is configured to perform the CRC calculation on a different number of bytes of data during a single cycle. Instead, and as noted above, Hyodo divides an input bit train into equal-length segments of data (e.g., five bits), each of which are input to a different one of the ROM tables (which may be considered "CRC modules" for the sake of argument only). By supplying equal-length segments of data to each of the ROM tables, the ROM tables of Hyodo each appear to be configured for performing a CRC calculation (by performing a look-up table operation; Hyodo, column 4, lines 27-32) on the same number of bits. This is altogether different from a plurality of CRC modules, where each of the CRC modules is configured to perform the CRC calculation on a different number of bytes. In fact, statements in the Office Action admit that "Hyodo does not explicitly teach the specific use of the various sized CRC circuits." (Office Action, page 11).

In addition, the process described by Hyodo fails to include the presently claimed step of determining which one of the plurality of CRC modules should be used for processing a segment of data currently supplied to the multiple-byte CRC circuit. Statements in the Office Action suggest that "Figure 6 in Hyodo teaches a means for determining which of the multiple cyclic redundancy check circuits is appropriate for the segment of data to be processed." (Office Action, page 9). The Applicant respectfully disagrees, for at least the reasons set forth in more detail below.

Hyodo discloses that "Fig. 6 is a block diagram of a ... synchronization circuit [for] handling input bit trains having indefinite time series", such as those shown in Fig. 5. *See*, e.g., Hyodo, column 5, lines 43-45 and Fig. 5. Hyodo also discloses that the synchronization circuit of Fig. 6 "includes a multiple stage shift register 12 and a CRC arithmetic unit 16 ... [which] is basically the same in circuit construction as the [CRC arithmetic unit] shown in ... Fig. 3." (Hyodo, column 5, lines 53-59). Thus, when an input bit train is supplied to the synchronization circuit of Fig. 6, the input bit train is shifted one bit at a time by each of the shift registers (12) to produce a plurality of equal-length data segments (each

comprising m-bits, as shown in Figs. 5 and 6). The m-bit data segments resulting from each shift (e.g., the q, q+1 and q+2 data segments of Fig. 5) are successively input to CRC arithmetic unit 16 for "executing a CRC arithmetic operation each time." *See*, Hyodo, column 5, lines 34-42. Hyodo provides absolutely no teaching or suggestion for determining which one of the ROM tables (the so-called "CRC modules) should be used for processing the m-bit data segments, once they are input to the CRC arithmetic unit (16). Therefore, Applicant's respectfully traverse the Examiner's suggestion that teaching or suggestion for the presently claimed step of determining can be found in Fig. 6 (or anywhere else) within Hyodo.

Since Hyodo fails to determine which one of the plurality of CRC modules should be used for processing a segment of data, Hyodo cannot be relied upon to provide teaching or suggestion for the presently claimed step of processing the segment of data using only the CRC module determined appropriate for the current segment of data.

For at least the reasons set forth above, Hyodo does not anticipate all limitations of independent claim 1. Therefore, claim 1 and all claims dependent therefrom are asserted to be patentably distinct over the cited art. Accordingly, Applicants respectfully request removal of this rejection.

Section 103 Rejections:

Claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hyodo in view of U.S. Patent No. 6,675,236 to Moon et al. (hereinafter "Moon"). In addition, claims 4 and 5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hyodo in view of U.S. Patent No. 6,530,057 to Kimmitt (hereinafter "Kimmitt"). To establish a case of *prima facie* obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (C.C.P.A 1974); MPEP 2143.03. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed.Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992); MPEP 2143.01. The cited art does not teach or suggest each and every limitation of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

Hyodo cannot be modified, or combined with Kimmitt or Moon, to provide teaching for a method of performing a cyclic redundancy check (CRC) calculation on a data stream, where the method includes: (i) supplying a data stream to a multiple-byte CRC circuit comprising a plurality of CRC modules, wherein each of the CRC modules is configured to perform the CRC calculation on a different number of bytes of data during a single cycle, (ii) determining which one of the plurality of CRC modules should be used for processing a segment of data currently supplied to the multiple-byte CRC circuit, and (iii) after said step of determining, processing the segment of data using only the CRC module determined appropriate for the current segment of data. As noted above in the § 102 arguments, Hyodo provides absolutely no teaching or suggestion for the aforementioned limitations of present claim 1. As described in more detail below, the teachings of Hyodo cannot be modified, or combined with those of Moon or Kimmitt, to provide teaching for the aforementioned limitations.

First of all, Hyodo cannot be modified to teach or suggest the aforementioned claim limitations, since Hyodo fails to suggest a desirability for doing so. The mere fact that references can be combined or modified does not render the resultant combination [or modification] obvious unless the prior art also suggests the desirability of the combination [or modification]. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); MPEP 2143.01. Unlike the presently claimed case, Hyodo fails to even suggest a desirability for determining which one of a plurality of CRC modules (where each is configured to perform a CRC calculation on a different number of bytes of data during a single cycle) should be used for processing a data segment, and then, for processing the data segment using only the CRC module determined to be appropriate. Furthermore, there is no teaching, suggestion or desirability within Hyodo for dividing the input bit train into anything other than equal-length data segments (e.g., m-bit segments). Therefore, Hyodo cannot be modified to provide teaching for the aforementioned limitations of present claim 1, since there is no motivation within the teachings of Hyodo to make such modification.

Kimmitt and Moon are not relied upon to provide teaching or suggestion for the aforementioned claim limitations. Since the primary reference to Hyodo fails to provide teaching for the aforementioned claim limitations, and the primary reference cannot be modified to do so, the primary reference cannot be combined with the remaining cited art in such a way that would provide teaching for the present claim limitations.

For at least the reasons set forth above, Hyodo cannot be modified or combined with the remaining cited art to teach or suggest all limitations of claim 1. Therefore, claim 1 and claims dependent therefrom are asserted to be patentably distinct over the cited art. Accordingly, Applicants respectfully request removal of this rejection.

Patentability of the Added Claims

The present amendment adds claims 11-20 which are dependent from claim 1. Therefore, claims 11-20 are patentably distinct over the cited art for at least the same reasons as claim 1. Accordingly, allowance of added claims 11-20 is respectfully requested.

CONCLUSION

The present amendment and response is believed to be a complete response to all issues raised in the Office Action mailed January 5, 2005. In view of the remarks traversing the rejections, Applicants assert that pending claims 1-5 and 11-20 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees which may be required, or credit any overpayment, to Daffer McDaniel, LLP Deposit Account No. 50-3268/5298-10900.

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